CLAIMS

1. A tuner comprising:
A phase-locked loop circuit;
a nonvolatile memory that stores alignment data,

2. The tuner of claim 1, wherein the alignment data can be utilized by the phase-locked loop.

3. The tuner of claim 1, wherein the nonvolatile memory is an EEPROM.

4. The tuner of claim 1, wherein the tuner is used in a television receiver.

5. The tuner of claim 4, wherein the tuner is coupled to a microprocessor, the microprocessor is contained in the television receiver.

6. The tuner of claim 1, wherein the phase-locked loop circuit is a phase-locked loop integrated circuit.

7. The tuner of claim 6, wherein the re-writable memory is integrated in the phase-locked loop integrated circuit.

8. The tuner of claim 6, wherein the re-writable memory is coupled to, but not integrated in, the phase-locked loop integrated circuit.

9. The tuner of claim 1, further comprising a D/A converter.

10. The tuner of claim 1, wherein the tuner further comprises an address decoder.

11. The tuner of claim 10, wherein the address decoder includes a 1 to 1 actual channel to alignment channel addressing scheme.

12. The tuner of claim 10, wherein the address decoder includes a plurality to 1 actual channel to alignment channel addressing scheme.

13. The tuner of claim 10, wherein the address decoder is implemented using software.

14. The tuner of claim 10, wherein the address decoder is implemented using hardware.

15. A television receiver comprising:
a microprocessor;
a first nonvolatile memory coupled to the microprocessor;
a tuner coupled to the microprocessor, the tuner comprising:
a phase-locked loop circuit coupled to the microprocessor, and
a second non-volatile memory.

16. The television receiver of claim 15, wherein the second nonvolatile memory is an EEPROM that can store alignment data.

17. A television control system for tuning a desired television signal, which comprises:
a radio frequency (RF) source for receiving an RF signal associated with television channels;
a tuner module, coupled to said RF source, for selecting the desired television signal from said RF signal, said tuner module having a memory unit, wherein said memory unit contains alignment data for said tuner module; and
a microprocessor, coupled to said tuner module, for communicating a tuning command corresponding to the desired television signal to said tuner module.

18. The television control system of claim 17 wherein said tuner module comprises:
a downconverter, coupled to said RF source, for selecting a RF signal corresponding to the desired television signal;
a phase-locked loop (PLL), coupled to said microprocessor and said downconverter, for receiving said tuning command and generating a frequency tone for output; and
an address decoder, coupled to said PLL and said memory unit, wherein said address decoder retrieves said alignment data from a memory location in said memory unit for the desired television signal.

19. The television control system of claim 17 wherein said microprocessor is coupled to said tuner module via an inter-integrated circuit bus.

20. The television control system of claim 17 wherein said memory unit comprises an electrically erasable programmable read only memory (EEPROM).

21. A television receiver for receiving a desired television signal, which comprises:

a radio frequency (RF) source for receiving an RF signal associated with television channels;

a tuner module, coupled to said RF source, for generating an RF signal corresponding to the desired television signal, said tuner module having a memory unit, wherein said memory unit contains alignment data for said tuner module;

an intermediate frequency (IF) module, coupled to said tuner module, for converting said RF signal corresponding with the desired television signal to an IF signal; and

a demodulation module, coupled to said IF module, for demodulation and display of the television information of the desired television signal.

22. The television receiver of claim 21 wherein said tuner module comprises:

a downconverter, coupled to said RF source, for selecting said RF signal corresponding to the desired television signal;

a phase-locked loop (PLL), coupled to said microprocessor and said downconverter, for generating a frequency tone for output; and

an address decoder, coupled to said PLL and said memory unit, wherein said address decoder retrieves said alignment data from a memory location in said memory unit for the desired television signal.

23. The television receiver of claim 21 wherein said said microprocessor is coupled to said tuner module via an inter-integrated circuit bus.

24. The television receiver of claim 21 wherein said memory unit comprises an electrically erasable programmable read only memory (EEPROM).